CLAIMS

What is claimed is:

1. A method of manufacturing a multilayer circuit board;

(a) applying a first continuous homogenous metal layer on a first dielectric layer,

(b) applying a first photoresist on said first metal layer;

(c) exposing and developing said first photoresist to define a conductive bump;

(d) etching the metal layer not covered by said first photoresist to reduce the height of said exposed metal layer and to provide said conductive bump;

(e) removing said first photoresist;

(f) applying a second photoresist onto said metal layer;

(g) exposing and developing said second photoresist to define a pattern comprising a conductive bump and a plurality of circuit lines;

(h) etching the metal layer exposed by the development of said second photoresist to form a conductive bump having an upper surface and a plurality of circuit lines in said metal layer;

(i) removing said second photoresist;

(j) forming an organic dielectric layer on the plurality of circuit lines and the substrate exposed by etching, said dielectric layer defining a hole which exposes the top surface of the conductive bump;

(k) applying a second metal layer onto said second dielectric layer and onto the exposed upper surface of said conductive bump to provide a multilayer substrate comprising a first metal layer and a second metal layer on opposing surfaces of said second dielectric layer, wherein said first metal layer and said second metal layer are interconnected by a solid conductive bump.

2. The method of claim 1 wherein said first metal layer comprises a plurality of conductive bumps, and said second metal layer has a substantially planar face, and further comprising the steps of:

(a) applying a third photoresist on said planar face;

(b) exposing and developing said third photoresist to define a plurality of conductive bumps;

(c) etching the metal layer exposed by development of said third photoresist to said exposed second metal layer to a second desired height;

(d) removing said third photoresist;

(e) applying a fourth photoresist onto said face of said second metal layer;

(f) exposing and developing said fourth photoresist to define a pattern

(g) etching the metal layer exposed by the development of said fourth photoresist to form a plurality of circuit lines in said metal layer; and

(h) removing said fourth photoresist to provide a printed circuit board comprising two conductive layers, each of said conductive layers comprising a plurality of conductive bumps and a plurality of circuit lines.

3. The method of claim 1 wherein the metal layer comprises copper.

4. The method of claim 1 wherein the etching step (d) comprises treating the exposed surface of the metal layer with an etching agent at less than 110°F for a time sufficient to reduce exposed portions of the metal layer to a desired second height and to produce said conductive bump.

5 The method of claim 4 wherein the etching agent is selected from the group consisting of cupric chloride, ferric chloride or sodium persulphate.

6. The method of claim 5 wherein the etching agent comprises cupric ions at a concentration of from about 125 to 225 gm/liter of etching agent.

7. The method of claim 1 wherein etching step (d) comprises forming said conductive bumps with a minimal undercut.

8. A method of forming a plurality of solid conductive bumps for interconnecting two conductive layers of a circuit board, said conductive bumps having upper surfaces, said method comprising the steps of

(a) obtaining a first continuous homogenous metal layer disposed on a second metal layer, said first metal layer having a substantially planar exposed face and said second metal layer having an exposed face;

(b) applying a first photoresist onto the exposed face of said first metal layer and a second photoresist onto the exposed face of said second metal layer;

(c) imaging said first photoresist to define a pattern of remaining photoresist sections;

(d) forming a plurality of conductive bumps by etching regions of the first metal layer not covered by said remaining first photoresist sections to a second desired height;

(e) removing said first photoresist and said second photoresist;

(f) applying a third photoresist onto the first metal layer and the second metal layer;

(g) exposing and developing said third photoresist on said first metal layer to define a pattern of conductive bumps and circuit lines;

(h) etching the first metal layer sections exposed by the development of said third photoresist to form a plurality of circuit lines in said first metal layer;

(i) removing said third photoresist;

(j) applying a dielectric layer onto said circuit lines, said dielectric layer defining a plurality of holes which expose the upper surfaces of said plurality of conductive bumps; and

(k) removing said second metal layer.

9. The method of claim 8 further comprising the step of applying a third conductive layer onto the dielectric layer to provide a structure comprising two metal

layers disposed on opposing surfaces of the dielectric, wherein said metal layers are interconnected by a plurality of solid conductive bumps.

10. The method of claim 9 wherein said first and said third metal layers comprise copper and said second metal layer comprises aluminum.

11. The method of claim 8 wherein the metal layer comprises copper.

12. The method of claim 8 wherein the etching step (d) comprises treating the exposed surface of the metal layer with an etching agent at less than 110°F for a time sufficient to reduce exposed portions of the metal layer to a desired second height and to produce said conductive bump.

13 The method of claim 12 wherein the etching agent is selected from the group consisting of cupric chloride, ferric chloride or sodium persulphate.

14. The method of claim 13 wherein the etching agent comprises cupric ions at a concentration of from about 125 to 225 gm/liter of etching agent.

15. The method of claim 8 wherein etching step (d) comprises forming said conductive bumps with a minimal undercut.

16. A method for fabricating a metallic border for providing rigidity to a panel, comprising:

(a) providing a continuous homogenous metal layer having a first height;

(b) applying a first photoresist to a face of said metal layer;

(c) exposing and developing said photoresist to provide at least one remaining photoresist section which defines an opening;

(d) etching the metal layer not covered by said remaining photoresist section to provide a region of metal having a second height;

(e) removing said remaining photoresist section to provide a metal border, said metal border having a first height and surrounding said region of metal having a second height.

17. The method of claim 16 further comprising the step of applying the metal layer to a dielectric substrate before step (b).

18. The method of claim 16 further comprising the step of applying the metal layer to a dielectric substrate after step (e).

19. The method of claim 16 wherein said photoresist is exposed and developed to provide first remaining photoresist section defining a hole and a second remaining photoresist section disposed within said hole; and wherein said etching further provides a conductive bump having a first height, said conductive bump being disposed on and continuous with said region of metal having a second height.